High Power, 44 W Peak, Silicon SPDT, Reflective Switch, 0.7 GHz to 3.5 GHz

Data Sheet **ADRF5130**

FEATURES

- Reflective, 50 Ω design
- Low insertion loss: 0.6 dB typical to 2.0 GHz
- High isolation: 50 dB typical to 2.0 GHz
- High power handling
  - RF input power, continuous wave (CW) at T_{CASE} = 85°C
    - 43 dBm maximum operating
    - 46.5 dBm absolute maximum rating
- High linearity
  - 0.1 dB compression (P0.1dB): 46 dBm typical
  - Input third-order intercept (IP3): 68 dBm typical to 2 GHz
- ESD ratings
  - Human body model (HBM): 2 kV, Class 2
  - Charged device model (CDM): 1.25 kV
- Single positive supply: V_{DD} = 5 V
- Positive control, TTL-compatible: V_{CTL} = 0 V or V_{DD}
- 24-lead, 4 mm × 4 mm LFCSP package (16 mm²)

APPLICATIONS

- Cellular/4G infrastructure
- Wireless infrastructure
- Military and high reliability applications
- Test equipment
- Pin diode replacement

FUNCTIONAL BLOCK DIAGRAM

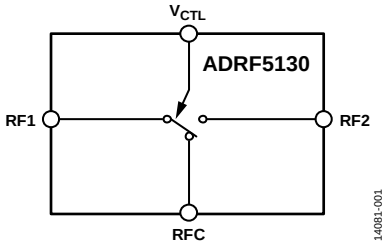

Figure 1.

GENERAL DESCRIPTION

The ADRF5130 is a high power, reflective, 0.7 GHz to 3.5 GHz, silicon, single-pole, double-throw (SPDT) switch in a leadless, surface-mount package. The switch is ideal for high power and cellular infrastructure applications, like long-term evolution (LTE) base stations. The ADRF5130 has high power handling of 43 dBm (maximum), a low insertion loss of 0.6 dB, input third-order intercept of 68 dBm (typical), and 0.1 dB compression (P0.1dB) of 46 dBm. On-chip circuitry operates at a single, positive supply voltage of 5 V and typical supply current of 1.06 mA, making the ADRF5130 an ideal alternative to pin diode-based switches.

The device comes in a RoHS compliant, compact, 24-lead, 4 mm × 4 mm LFCSP package.

Rev. B

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REVISION HISTORY

5/2018—Rev. A to Rev. B

Change to RFC to RF2 Column, Table 5 7
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1/2017—Rev. 0 to Rev. A

Changes to Ordering Guide 10

7/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V, V_{CTL} = 0 V or V_{DD}, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.7		3.5	GHz
INSERTION LOSS		0.7 GHz to 2.0 GHz		0.6		dB
		2.0 GHz to 3.5 GHz		0.7		dB
ISOLATION						
RFC to RF1 or RF2 (Worst Case)		0.7 GHz to 2.0 GHz		50		dB
		2.0 GHz to 3.5 GHz		46		dB
RF1 to RF2 (Worst Case)		0.7 GHz to 2.0 GHz		51		dB
		2.0 GHz to 3.5 GHz		41		dB
RETURN LOSS						
RFC		0.7 GHz to 2.0 GHz		23		dB
		2.0 GHz to 3.5GHz		17		dB
RFC to RF1 or RF2		0.7 GHz to 2.0 GHz		21		dB
		2.0 GHz to 3.5 GHz		17		dB
SWITCHING SPEED						
Time						
Rise and Fall	t_{RISE}, t_{FALL}	90% to 10% of RF output		155		ns
On and Off	t_{ON}, t_{OFF}	50% V_{CTL} to 10% to 90% of RF output		750		ns
RADIO FREQUENCY (RF) SETTLING TIME		50% V_{CTL} to 0.1 dB margin of final RF output		1.8		µs
INPUT POWER						
0.1 dB Compression	P0.1dB			46		dBm
INPUT THIRD-ORDER INTERCEPT	IP3	Two-tone input power = 25 dBm/tone				
		0.7 GHz to 2 GHz		68		dBm
		2 GHz to 3.5 GHz		65		dBm
RECOMMENDED OPERATING CONDITIONS		0.7 GHz to 3.5 GHz				
Voltage Range						
Bias	V_{DD}		4.5		5.4	V
Control	V_{CTL}		0		V_{DD}	V
Maximum RF Input Power						
T_{CASE} = 105°C		Continuous wave			41	dBm
T_{CASE} = 85°C		Continuous wave			43	dBm
		8 dB peak to average ratio (PAR) LTE, average			38	dBm
		8 dB PAR LTE, single event (<10 sec), average			44	dBm
T_{CASE} = 25°C		Continuous wave			44.5	dBm
Case Temperature Range	T_{CASE}		−40		+105	°C
DIGITAL INPUT CONTROL VOLTAGE		V_{DD} = 4.5 V to 5.4 V, T_{CASE} = −40°C to +105°C at <1 µA typical				
Low Range	V_{IL}		0		0.8	V
High Range	V_{IH}		1.3		5.0	V
SUPPLY CURRENT	I_{DD}	V_{DD} = 5 V		1.06		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Bias Voltage Range (V_{DD})	−0.3 V to +5.5 V
Control Voltage Range (V_{CTL})	−0.3 V to +5.5 V
RF Input Power,[1] Continuous Wave	46.5 dBm
Channel Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +105°C
Peak Reflow Temperature (MSL3)[2]	260°C
Thermal Resistance (Channel to Package Bottom)	17°C/W
Electrostatic Discharge (ESD) Sensitivity	
HBM	2 kV (Class 2)
CDM	1.25 kV

[1] For the recommended operating conditions, see Table 1.
[2] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

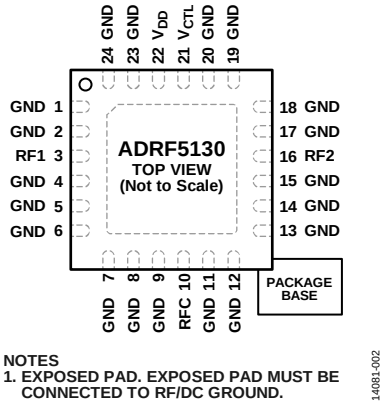


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 9, 11 to 15, 17 to 20, 23, 24	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF/dc ground. See Figure 3 for the GND interface schematic.
3	RF1	RF Output Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
10	RFC	RF Input Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
16	RF2	RF Output Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
21	V_{CTL}	Control Input. See Figure 4 for the V_{CTL} interface schematic. Refer to Table 4 and the recommended digital input control voltage range in Table 1.
22	V_{DD}	Supply Voltage. See Figure 4 for the V_{DD} interface schematic.
	EPAD	Exposed Pad. Exposed pad must be connected to RF/dc ground.

Table 4. Truth Table

	Signal Path State	
Control Input (V_{CTL}) State	**RFC to RF1**	**RFC to RF2**
Low	Off	On
High	On	Off

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

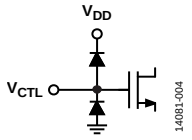


Figure 4. Control Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, RETURN LOSS, AND IP3

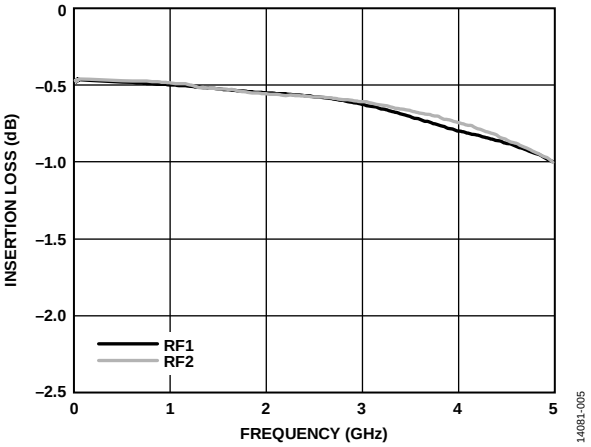


Figure 5. Insertion Loss of RF1 and RF2 vs. Frequency at V_{DD} = 5 V

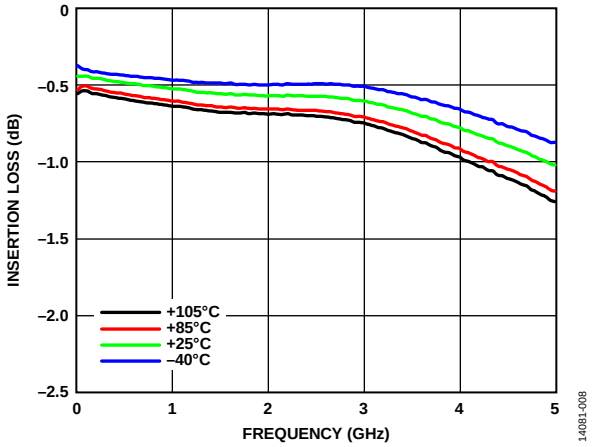


Figure 8. Insertion Loss vs. Frequency over Temperature at V_{DD} = 5 V

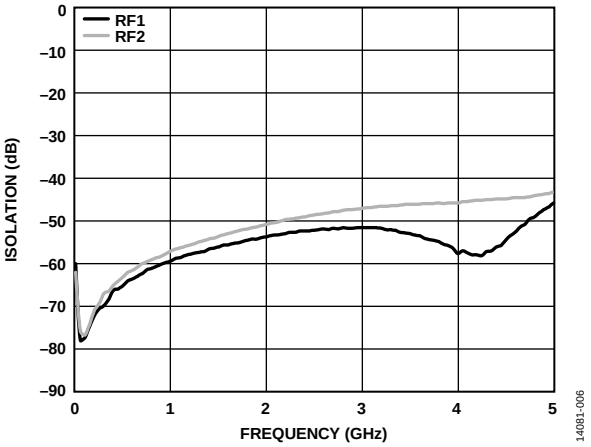


Figure 6. Isolation Between RFC to RF1 or RF2 vs. Frequency at V_{DD} = 5 V

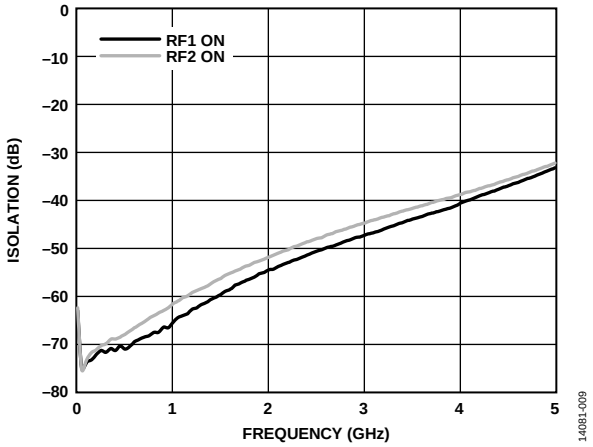


Figure 9. Isolation Between RF1 and RF2 vs. Frequency at V_{DD} = 5 V, Switch Mode On

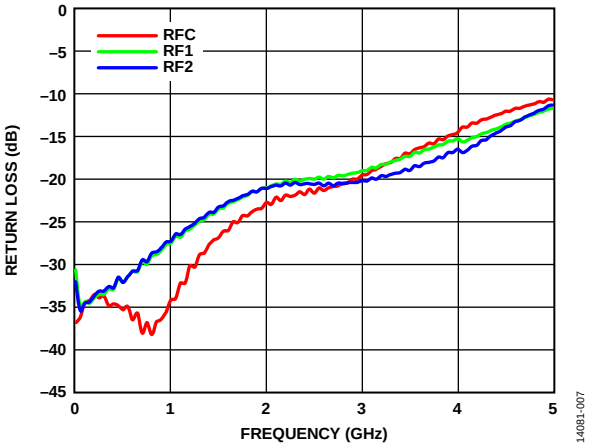


Figure 7. Return Loss vs. Frequency at V_{DD} = 5 V (RFC, RF1, and RF2)

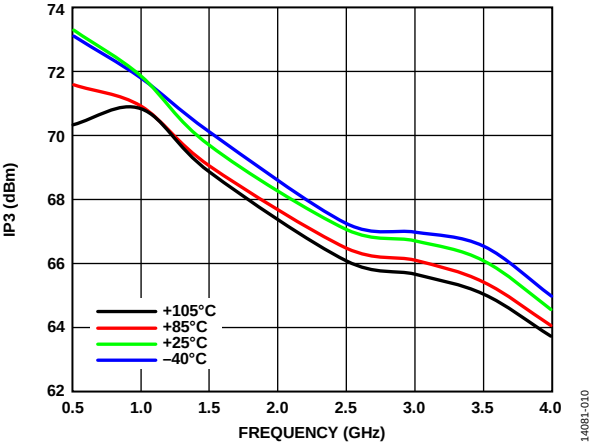


Figure 10. IP3 vs. Frequency over Temperature, V_{DD} = 5 V

THEORY OF OPERATION

The ADRF5130 requires a single-supply voltage applied to the V_{DD} pin. Bypass capacitors are recommended on the supply line to minimize RF coupling.

A digital control voltage applied to the V_{CTL} pin controls the ADRF5130. A small bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The ADRF5130 is internally matched to 50 Ω at the RF input port (RFC) and the RF output ports (RF1 and RF2); therefore, no external matching components are required. The RFx pins are dc-coupled, and dc blocking capacitors are required on the RF lines. The design is bidirectional; the input and outputs are interchangeable.

The ideal power-up sequence of the ADRF5130 is as follows:

1. Connect to GND.
2. Power up V_{DD}.
3. Power up the digital control input. Powering the digital control input before the V_{DD} supply can inadvertently forward-bias and damage the ESD protection structures.
4. Power up the RF input. Depending on the logic level applied to the V_{CTL} pin, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from the input to the output, while the other RF output port (for example, RF2) is set to off mode, by which the output is isolated from the input.

Table 5. Switch Operation Mode

	Switch Mode	
Digital Control Input (V_{CTL})	**RFC to RF1**	**RFC to RF2**
0	Off mode: the RF1 port is isolated from the RFC port and is internally terminated to a 50 Ω load to absorb the applied RF signals.	On mode: a low insertion loss path from the RFC port to the RF2 port.
1	On mode: a low insertion loss path from the RFC port to the RF1 port.	Off mode: the RF2 port is isolated from the RFC port and becomes open reflective.

APPLICATIONS INFORMATION

Generate the evaluation PCB used in the application circuit shown in Figure 11 with proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and backside ground slug must connect directly to the ground plane, as shown in Figure 14.

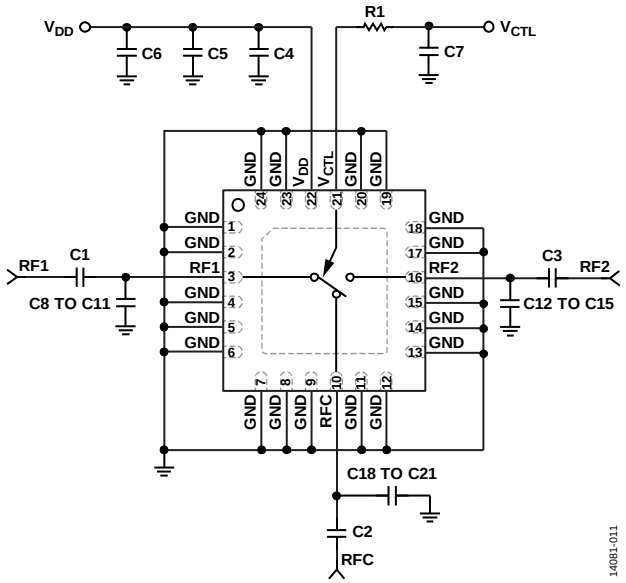


Figure 11. Application Circuit

EVALUATION BOARD

The ADRF5130 evaluation board has eight metal layers and dielectrics between each layer (see Figure 12). The top and the bottom metal layers have copper thickness of 2 oz (2.7 mil), whereas the metal layers in between them have 1 oz copper (1.3 mil) thickness. The top dielectric material is 10 mil Rogers RO4350, which exhibits a very low thermal coefficient, offering control over thermal rise of the board. The dielectrics between other metal layers are FR-4. The overall board thickness achieved is 62 mil.

Figure 13 shows the top view of the ADRF5130 evaluation board.

The top copper layer has all RF and dc traces, whereas the other seven layers provide good ground and help to handle the thermal rise on the evaluation board caused by the high power of the ADRF5130. In addition, for proper thermal grounding, many via holes are provided around the transmission lines and under the exposed pad of the package. RF transmission lines on the ADRF5130 evaluation board are coplanar wave guide design with an 18 mil width and a ground spacing of 13 mil. For controlling the thermal rise of the ADRF5130 evaluation board at high temperatures and power levels, it is recommended to use a heat sink and a mini dc fan.

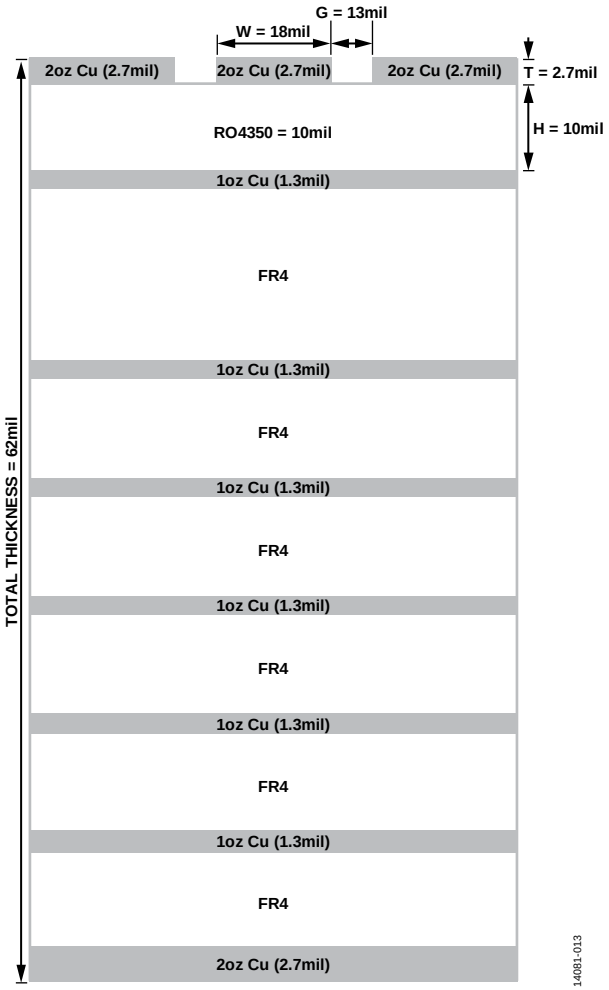


Figure 12. Evaluation Board Cross-Sectional View

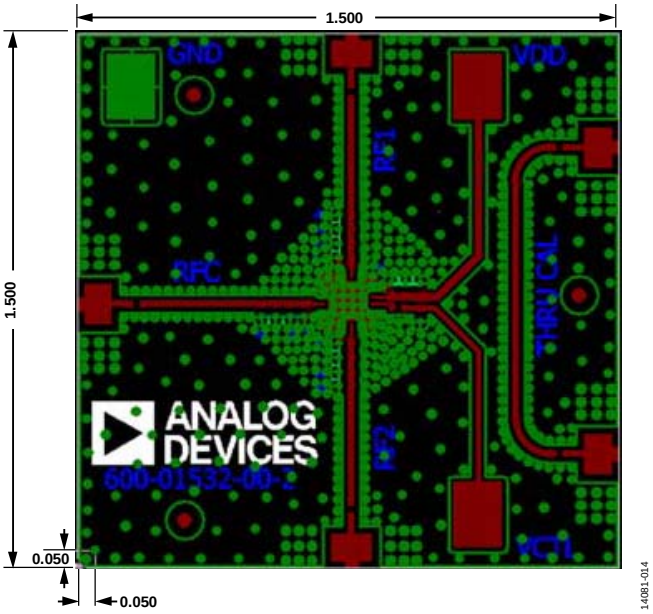


Figure 13. Evaluation Board Top View

Figure 14 shows the ADRF5130 evaluation board with all components populated. The VDD supply port connects to TP1. The VDD supply trace has three bypass capacitors 100 pF, 1 µF, and 1 nF. The TP2 test point connects to the control voltage port (VCTL). The control trace has a 100 pF bypass capacitor and 0 Ω resistor. The ground reference connects to GND. A 100 pF dc blocking capacitor is used on all RF traces that connect the RF1, RF2, and RFC ports to the J1, J2, and J3 connectors, respectively. The connectors used are 2.9 mm end launch SMA connectors. Unpopulated capacitor positions are available on all RF traces to provide extra matching. A through transmission line (THRU CAL) is available on the ADRF5130 evaluation board that can measure board loss on the printed circuit board (PCB).

Table 6 shows the bill of materials for the ADRF5130 evaluation board. The evaluation board shown in Figure 14 is available from Analog Devices, Inc., upon request.

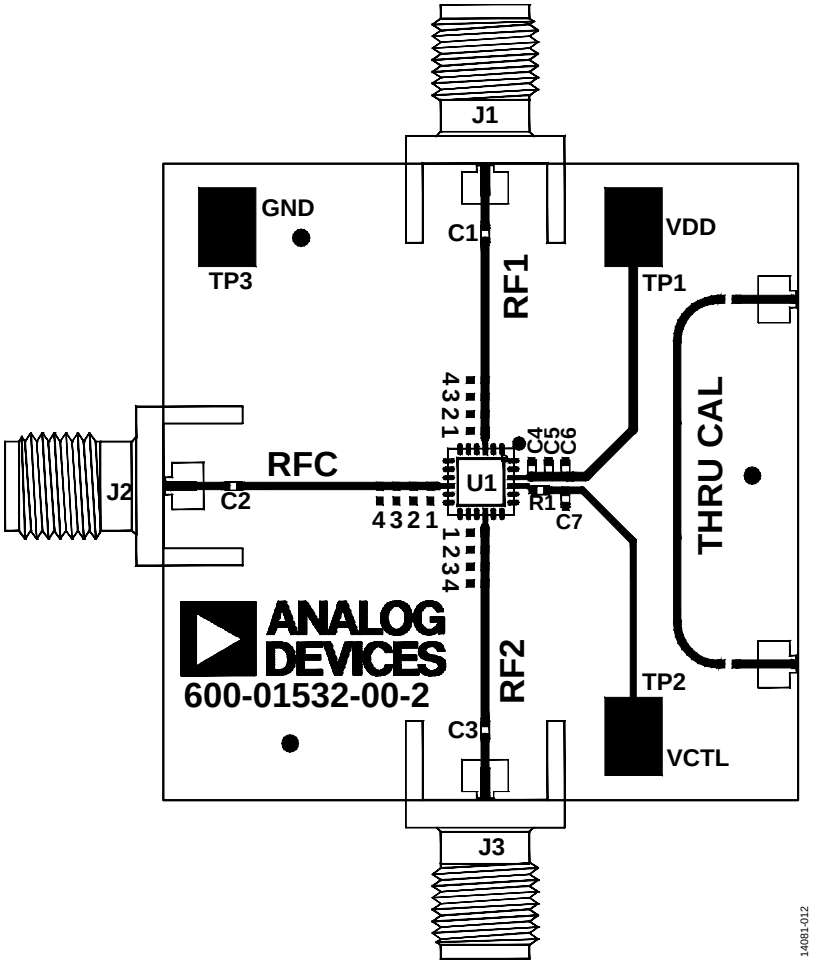


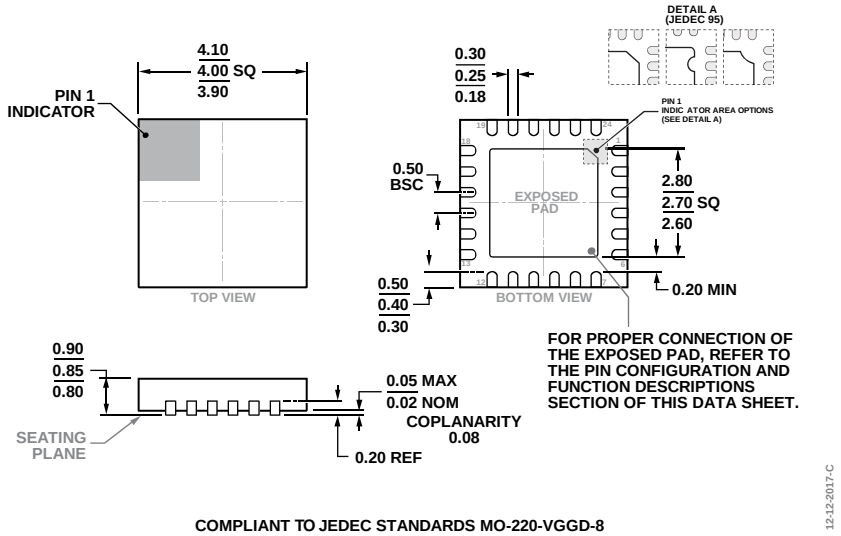
Figure 14. ADRF5130-EVALZ Evaluation Board

Table 6. Bill of Materials for the ADRF5130-EVALZ Evaluation Board

Reference Designator	Description
J1 to J3	PCB mount SMA connectors
C1 to C4, C7	100 pF capacitors, 0402 package
C5	1 nF capacitor, 0402 package
C6	1 µF capacitor, 0402 package
C8 to C15, C18 to C21	Do not insert (DNI)
R1	0 Ω resistor, 0402 package
TP1, TP2, TP3	Surface-mount test points
U1	ADRF5130 SPDT switch
PCB	600-01532-00-2[1] evaluation PCB; circuit board material: Rogers RO4350 or Arlon 25FR

[1] Reference this evaluation board number when ordering the complete evaluation board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 15. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.85 mm Package Height
(CP-24-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
ADRF5130BCPZ	−40°C to +105°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-16
ADRF5130BCPZ-R7	−40°C to +105°C	MSL3	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-16
ADRF5130-EVALZ	−40°C to +105°C		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section.

D14081-0-5/18(B)

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